

<b>Notice of References Cited</b>	Application/Control No. 10/709,205		Applicant(s)/Patent Under Reexamination BONGES ET AL.	
	Examiner Helen Rossoshek		Art Unit 2825	Page 1 of 2

#### U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,282,696 B1	08-2001	Garza et al.	716/19
*	B	US-6,324,673 B1	11-2001	Luo et al.	716/11
*	C	US-2003/0023939 A1	01-2003	Pierrat et al.	716/3
*	D	US-6,557,162 B1	04-2003	Pierrat	716/21
*	E	US-6,560,766 B2	05-2003	Pierrat et al.	716/19
*	F	US-2004/0078724 A1	04-2004	Keller et al.	714/048
*	G	US-6,769,102 B2	07-2004	Frank et al.	716/5
*	H	US-2004/0210856 A1	10-2004	Sanie et al.	716/002
*	I	US-6,845,034 B2	01-2005	Bhattacharyya	365/149
*	J	US-2005/0076316 A1	04-2005	Pierrat et al.	716/004
*	K	US-6,901,574 B2	05-2005	LaCour et al.	716/19
*	L	US-6,931,617 B2	08-2005	Sanie et al.	716/18
*	M	US-7,017,141 B2	03-2006	Anderson et al.	716/19

#### FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

#### NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Bhat et al., "Special Purpose Architecture for Accelerating Bitmap DRC", 25-29 June 1989, Design Automation, 26th Conference on, Page(s):674 - 677□□
	V	Rutenbar et al., "A Class of Cellular Architectures to Support Physical Design Automation", October 1984, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Volume 3, Issue 4, Page(s):264 - 278
	W	Eustace et al., "A Deterministic Finite Automaton Approach to Design Rule Checking for VLSI", 14-16 June 1982, Design Automation, 19th Conference on, Page(s):712 - 717□□
	X	Schaffer et al., "Requirements and constraints for the design of smart photodetector arrays for page-oriented optical memories", Sept.-Oct. 1998, Selected Topics in Quantum Electronics, IEEE Journal of, Volume 4, Issue 5, Page(s):856 - 865 □□

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<b>Notice of References Cited</b>	Application/Control No. 10/709,205	Applicant(s)/Patent Under Reexamination BONGES ET AL.	
	Examiner Helen Rossoshek	Art Unit 2825	Page 2 of 2

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,263,299 B1	07-2001	Aleshin et al.	703/5
*	B	US-6,317,859 B1	11-2001	Papadopoulos	716/4
*	C	US-6,535,247 B1	03-2003	Kozlowski et al.	348/241
*	D	US-6,629,292 B1	09-2003	Corson et al.	716/3
*	E	US-6,615,393 B1	09-2003	Bell, Risto	716/5
*	F	US-6,856,030 B2	02-2005	Madurawe	257/141
*	G	US-6,917,380 B1	07-2005	Tay	348/247
*	H	US-6,917,041 B2	07-2005	Doty et al.	250/370.09
*	I	US-2005/0216877 A1	09-2005	Pack et al.	716/019
*	J	US-2005/0273748 A1	12-2005	Hetzel et al.	716/014
*	K	US-6,996,797 B1	02-2006	Liebmann et al.	716/19
*	L	US-6,998,722 B2	02-2006	Madurawe	257/66
*	M	US-7,030,651 B2	04-2006	Madurawe,	326/41

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Seiler, "A Hardware Assisted Design Rule Check Architecture", 14-16 June 1982, Design Automation, 19th Conference on Page(s):232 - 238
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.